WHAT IS CLAIMED IS:

1. A method of fault correction for an array of fusible links, comprising the steps of:

providing a first plurality of fusible links;

providing a second plurality of fusible links;

storing digital information in said first plurality of fusible links to place said first plurality of fusible links in a first programmed state;

storing said digital information in said second plurality of fusible links to place said second plurality of fusible links in a second programmed state, said first programmed state and said second programmed state being identical in an absence of a faulty bit in one of said first plurality of fusible links and said second plurality of fusible links; and

performing a logic operation to combine said first programmed state with said second programmed state, said logic operation providing an output that is identical to one of said first programmed state and said second programmed state for a respective one of said first plurality of fusible links and said second plurality of fusible links that does not include said faulty bit.

2. The method of claim 1, wherein said logic operation is one of an AND operation and an OR operation.

3. The method of claim 1, comprising the step of performing a further logic operation that compares said first programmed state with said second programmed state to determine a position of a faulty bit for said first plurality of fusible links and said second plurality of fusible links.

4. The method of claim 3, wherein said further logic operation is an exclusive-OR operation.

5. The method of claim 3, wherein a threshold is set that identifies a maximum number of bits that can be faulty before said array of fusible links is deemed unusable.

6. The method of claim 1, further comprising the step of providing a circuit which determines that at least one fusible link of said first plurality of fusible links and said second plurality of fusible links has been opened when said at least one fusible link has a resistance in a range of about 1k ohms to about 2k ohms.

7. The method of claim 1, further comprising the step of providing a circuit which determines that at least one fusible link of said first plurality of fusible links and said second plurality of fusible links has been opened when said at least one fusible link has a resistance in a range of about 1k ohms to about 30k ohms.

8. The method of claim 1, further comprising the step of providing a circuit which determines that at least one fusible link of said first plurality of fusible links and said second plurality of fusible links has been opened when said at least one fusible link has a resistance of at least about 1k ohms.

9. The method of claim 1, further comprising the step of providing a circuit which determines that a fusible link has been opened when a read current through said fusible link is about ten percent or less of a write current used to open said fusible link.

10. The method of claim 1, said method being implemented in at least one of an ink jet printhead and an ink jet printer.

11. The method of claim 1, each of said first plurality of fusible links and said second plurality of fusible links having a common plurality of bit positions, wherein in said performing step if each of said first plurality of fusible links and said second plurality of fusible links include at least one faulty bit, said logic operation providing an output that is identical to said digital information, so long as a bit position of a first faulty bit in said first plurality of fusible links does not correspond to a bit position of a second faulty bit in said second plurality of fusible links.

12. A sense circuit for reading a fusible link, comprising:

a first transistor defining a read input for receiving a read signal, a first terminal coupled to said fusible link, and a second terminal coupled to an output port; and

a second transistor having a bias input biased to a voltage reference, having a third terminal coupled to said second terminal of said first transistor, and a fourth terminal coupled to a ground.

13. The sense circuit of claim 12, further comprising an inverter circuit coupled between said second terminal of said first transistor and said output port.

14. The sense circuit of claim 12, wherein an output voltage at said output port in a range of about 1 volt to about 2.5 volts signifies that said fusible link is opened.

15. The sense circuit of claim 12, wherein an output voltage at said output port of about 1.5 volts signifies that said fusible link is opened.

16. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance in a range of about 1k ohms to about 2k ohms.

17. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance in a range of about 15k ohms to about 30k ohms.

18. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance of about 1k ohms.

19. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance of about 2k ohms.

20. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance of about 17k ohms.

21. The sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance of about 27k ohms.

22. The sense circuit of claim 12, further comprising a third transistor having an input terminal coupled to said voltage reference, having a fifth terminal coupled between said fusible link and said first terminal of said first transistor, and having a sixth terminal coupled to ground.

23. The sense circuit of claim 12, said sense circuit being incorporated in at least one of an ink jet printhead and an ink jet printer.

24. A printhead comprising an array of fusible links, said array of fusible links including a first plurality of fusible links and a second plurality of fusible links, said first plurality of fusible links being redundant with respect to said second plurality of fusible links.

25. The printhead of claim 24, further comprising a circuit for programming digital information into said array of fusible links.

26. The printhead of claim 24, further comprising a circuit for reading digital information from said array of fusible links.